A 60-GHz-Band Monolithic HJFET LNA Incorporating a Diode-Regulated Self-Bias Circuit

Kenichi Maruhashi, *Member, IEEE,* Keiichi Ohata, *Member, IEEE,* and Mohammad Madihian, *Senior Member, IEEE*

***Abstract*— This paper presents a 60-GHz-band GaAs heterojunction FET (HJFET) low-noise amplifier (LNA) operating with a single bias supply. A diode-regulated self-bias circuit was incorporated for suppressing the FET drain–current variations due to threshold voltage nonuniformities. The effect of the bias circuit on the drain–current distribution is carefully discussed based on the FET dc characteristics. A developed three-stage monolithic microwave integrated circuit (MMIC) LNA exhibited an average noise figure of 3.3 dB with 18-dB gain from 58 to 62 GHz. The LNA could operate over 2–5 V with a constant noise figure. The LNA chip size is 1.85 mm $\times$ 1.07 mm.**

***Index Terms*— Amplifier noise, millimeter-wave amplifiers, millimeter-wave integrated circuits, MMIC's, MODFET amplifiers.**

I. Introduction

TO DATE, several applications such as wireless local-area amplifiers (LAN's), cordless cameras, and contactless ID card systems [1] have been proposed and tested for 60-GHz frequency band. A monolithic microwave integrated circuit (MMIC) low-noise amplifier (LNA) is a key element for low-cost *RX* modules in the above-mentioned systems. A self-biased LNA is useful because it requires only one positive voltage source and simplifies bias networks for MMIC design. Recently, self-biased MMIC LNA's have been reported at C- and X-bands [2]–[4]. However, to our knowledge, there have been no reports for single-bias monolithic LNA's operating at higher frequency bands. In addition, for a high transconductance millimeter-wave heterojunction FET (HJFET), the drain current is sensitive to threshold voltage variations due to nonuniformities in the wafers and the gate recess process. In an example of a single-stage V-band LNA when the drain current is changed over a range of 5 ± 2 mA for a 60-μm gatewidth HJFET, noise figure and gain deviate by 0.3 and 1.3 dB, respectively. For a self-biased LNA, a current regulation is a first step approaching to high manufacturability and low-cost production. As a technique to reduce the threshold voltage variations, a selective gate recess process is used. However, for a short gate-length low-noise device it is not mature so far because of the damage by dry etching or the less recess width controllability by wet etching.

Manuscript received March 31, 1997; revised August 15, 1997.

K. Maruhashi and K. Ohata are with Kansai Electronics Research Laboratory, NEC Corporation, Otsu, Shiga 520 Japan.

M. Madihian is with C&C Media Research Laboratories, NEC Corporation, Miyamae-ku, Kawasaki 216 Japan (e-mail: maru@kel.cl.nec.co.jp).

Publisher Item Identifier S 0018-9480(97)08360-9.

This paper describes a small-size 60-GHz-band MMIC LNA operating with a single bias supply, based on 0.15-μm AlGaAs/InGaAs HJFET technologies. A simple self-bias circuit is considered for a millimeter-wave monolithic LNA in Section II. Incorporating a diode-regulated self-bias circuit, the drain–current variation mainly due to the FET threshold voltage ($V_{\rm th}$) nonuniformities is reduced to 58% compared to that for a conventional gate-grounded bias circuit. In Sections III and IV, LNA circuit design, fabrication process, and device characteristics are presented. Section V demonstrates the developed LNA noise performance as a function of supply voltage and temperature, and Section VI presents a conclusion.

II. Self-Bias Circuit Consideration for LNA

There are two kinds of self-bias circuits: active and passive. An active self-bias circuit can regulate the current more precisely incorporating active elements [3], such as HEMT's. However, it requires relatively large area, needs biasing itself, demands a higher voltage than that for the FET in the amplifier circuit, and causes yield problems especially for millimeter-wave MMIC's. This paper, therefore, applies a passive self-bias circuit.

Practical passive networks including a diode-regulated self-bias circuit proposed here, a gate-grounded circuit, and a resistive self-bias circuit are shown in Fig. 1(a)–(c), respectively. All circuits incorporate resistors (R) between source terminals and the ground, which cause the FET's under-depletion mode. These resistors act as feedback elements helping regulate the drain current. In the diode-regulated self-bias circuit [Fig. 1(a)], a current limiting resistor and the diode are connected in series between the source terminal of the FET and the ground. As an alternative configuration, a set of these elements can be connected between the drain voltage ($V_{\rm d}$) and the ground. However, we did not employ the latter because of layout complexity due to the connection between gate- and drain-bias circuits. A Schottky diode forward turn-on voltage ($V_{\rm f}$) is applied to the gate voltage ($V_{\rm g} = V_{\rm f}$), while $V_{\rm g} = 0$ for the gate-grounded self-bias circuit [Fig. 1(b)]. For these two cases, the drain current ($I_{\rm d}$) weakly depends on $V_{\rm d}$ due to the constant $V_{\rm g}$. In other words, a designed amplifier can be operated at a relatively wide supply voltage range with a low noise current condition. On the contrary, in the resistive self-bias circuit [Fig. 1(c)], $V_{\rm g}$ is a function of $V_{\rm d}$, resulting in a significant $I_{\rm d}$ variation when the $V_{\rm d}$ changes. The resistive self-bias circuit requires a bias line from drain- (dc pad) to

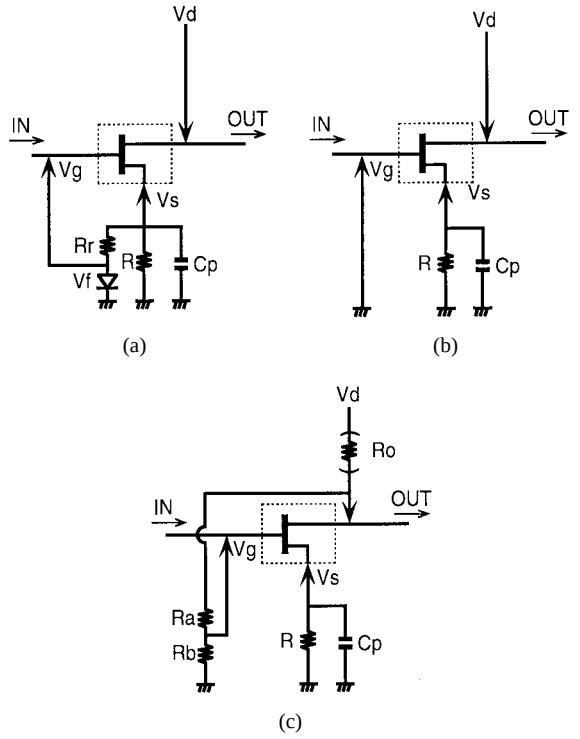

Fig. 1. Practical passive self-bias circuits for a depletion-mode FET. (a) Diode-regulated, (b) gate-grounded, and (c) resistive circuits.

gate-bias circuits across an RF signal line in a compact layout for MMIC design, which causes layout complexity. Thus, in the following we focus on the diode-regulated self-bias circuit with the gate-grounded self-bias circuit as a reference. Based on the FET dc characteristics, the drain–current variation is described.

The drain current for a low noise current condition (near pinchoff region) is approximately described as

$$I_{\rm d} = \beta(V_{\rm g} - V_{\rm s} - V_{\rm th})^2 \sim \beta(V_{\rm g} - R \cdot I_{\rm d} - V_{\rm th})^2 \quad (1)$$

where $V_{\rm s}$ is the source voltage and β is a fitting factor. The curves $(\sqrt{I_{\rm d}}, V_{\rm gs})$ for the HJFET's with different $V_{\rm th}$'s are plotted in Fig. 2. At a range from 2.5 to 7.5 mA for a 60-μm HJFET, each curve is well fitted with a linear plot, which implies that (1) is appropriate. It should be noted that β (derived from slopes) is independent of $V_{\rm th}$ over the threshold voltage variation of 0.5 V, as shown in Fig. 3, in which the β's for different HJFET's are plotted.

The drain current is deduced as

$$I_{\rm d} = \frac{V_{\rm g} - V_{\rm th}}{R} + \frac{1}{2\beta R^2}\left[1 - \sqrt{1 + 4\beta R(V_{\rm g} - V_{\rm th})}\right]. \quad (2)$$

We define a drain–current sensitivity to the FET threshold voltage as follows:

$$\frac{\partial I_{\rm d}}{\partial V_{\rm th}} = -\frac{1}{R}\left[1 - \frac{1}{\sqrt{1 + 4\beta R(V_{\rm g} - V_{\rm th})}}\right]. \quad (3)$$

Since the transconductance including the resistor ($G_m^{\rm EXT}$) is equal to $-(\partial I_{\rm d})/(\partial V_{\rm th})$ [2], the drain–current sensitivity is also expressed as $-G_m/(1 + R \cdot G_m)$, where G_m is an FET transconductance without the resistor. Thus, R is an important

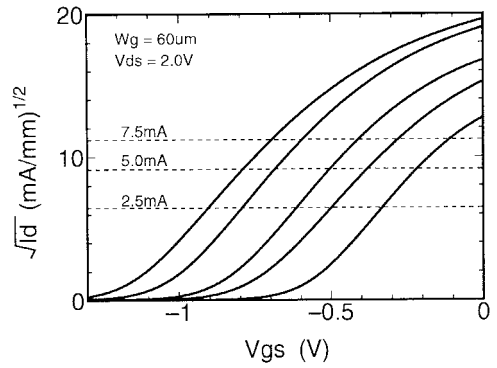

Fig. 2. $(\sqrt{I_{\rm d}}, V_{\rm gs})$ curves for HJFET's with different threshold voltages.

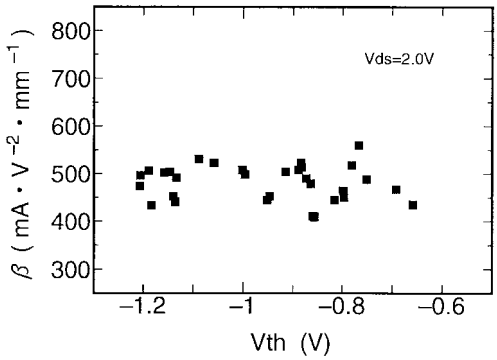

Fig. 3. The β parameters for HJFET's with different threshold voltages.

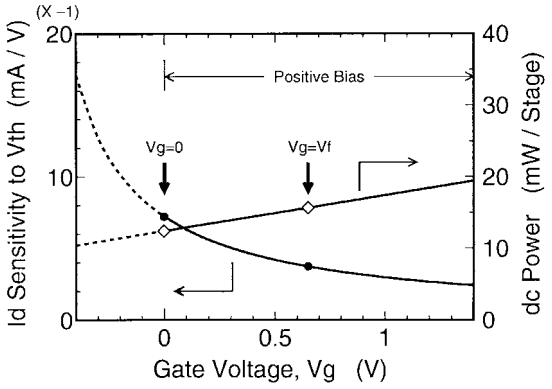

Fig. 4. Drain–current sensitivity to threshold voltage variation, and dc power consumption as a function of gate voltage for a self-biased single-stage amplifier.

factor to determine the drain–current sensitivity. For a set drain current ($I_{\rm d}^{\rm SET}$), R is represented from (1) as

$$R = \frac{1}{I_{\rm d}^{\rm SET}}\left(V_{\rm g} - V_{\rm th} - \sqrt{\frac{I_{\rm d}^{\rm SET}}{\beta}}\right). \quad (4)$$

From (3) and (4), the drain–current sensitivity as a function of $V_{\rm g}$ can be calculated as shown in Fig. 4, with dc consumption power for one stage. The employed parameters are $\beta = 28.8$ mA/V^2, $I_{\rm d}^{\rm SET} = 5$ mA, and $V_{\rm th}$ (typical) $= -0.9$ V for the 60-μm HJFET and $V_{\rm f} = 0.65$ V for the diode. The drain–current sensitivity to the threshold voltage for the diode-regulated circuit ($V_{\rm g} = 0.65$ V and $R = 227\ \Omega$) corresponds to $\pm 15\%$

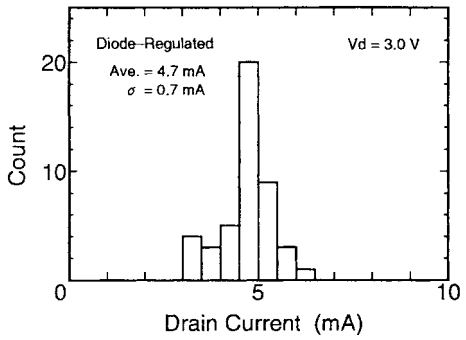

Fig. 5. Drain–current distributions over a wafer for (a) the diode-regulated and (b) the gate–grounded self-bias circuits.

TABLE I
MEASURED AND CALCULATED STANDARD DEVIATIONS FOR DRAIN CURRENT OVER A WAFER ($W_g = 60\ \mu m$)

Parameter	Parameter Value	σ Contributed by Parameter			
		Measured		Calculated	
	Typical ($\pm\sigma$)	Diode-Regulated	Gate-Grounded	Diode-Regulated	Gate-Grounded
Vth	-0.90 (± 0.17) V	—	—	0.64 mA	1.24 mA
β	28.8 (± 2.3) mA·V^{-2}	—	—	0.06 mA	0.12 mA
R	118 (± 7) Ω/□	—	—	0.25 mA	0.21 mA
Total	—	0.69 mA	1.18 mA	0.69 mA	1.26 mA

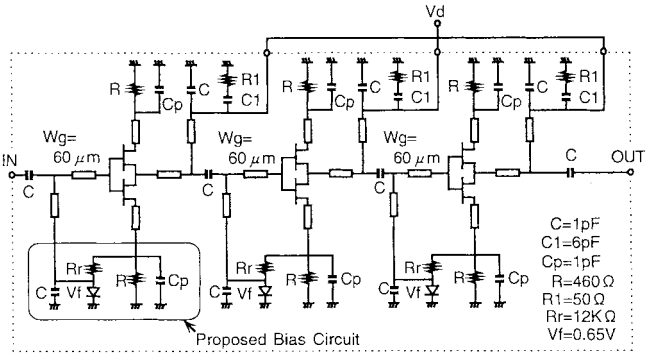

Fig. 6. Circuit topology for the designed self-biased three-stage monolithic LNA.

current variation over a ±0.2-V threshold voltage deviation, and is 52% of that for the gate–grounded circuit ($V_g = 0$ and $R = 97\ \Omega$), while dc consumption power is acceptably increased by 26%. From (2), the drain current sensitivities to β and R are calculated as

$$\frac{\partial I_d}{\partial \beta} = -\frac{1}{2\beta^2 R^2}\left[1 - \frac{1 + 2\beta R(V_g - V_{th})}{\sqrt{1 + 4\beta R(V_g - V_{th})}}\right] \tag{5}$$

$$\frac{\partial I_d}{\partial R} = -\frac{V_g - V_{th}}{R^2} - \frac{1}{\beta R^3}\left[1 - \frac{1 + 3\beta R(V_g - V_{th})}{\sqrt{1 + 4\beta R(V_g - V_{th})}}\right]. \tag{6}$$

The drain–current distributions evaluated on a 3-in wafer are shown in Fig. 5(a) and (b). The standard deviation of the drain current (σ) for the diode-regulated self-bias circuit was reduced to 58% compared to that for the gate–grounded circuit. For the reduction, the current criterion of ±2 mA was satisfied with 2.9σ. The measured and calculated drain–current distributions are summarized in Table I. The standard deviations of $\sigma_{V_{th}}$, σ_β, and σ_R contributed by V_{th}, β, and R are calculated using (3), (5), and (6). Total σ is derived from $\sqrt{\sigma_{V_{th}}^2 + \sigma_\beta^2 + \sigma_R^2}$ for the calculation since β is independent of V_{th}, as previously mentioned. The contribution by the V_f variation to σ is negligible because it is one order lower than that by the V_{th} variation. It is clearly confirmed that the main parameter contributing to the I_d distribution is the V_{th}. The calculated σ for the diode-regulated circuit is 55% compared to that for the gate–grounded circuit, which agrees well with the measured data.

III. AMPLIFIER CIRCUIT DESIGN

A circuit topology for the designed monolithic three-stage LNA is shown in Fig. 6. In the circuit, 0.15-μm AlGaAs/InGaAs HJFET's were employed. The Pospieszalski noise model [5] was used for the HJFET with $T_g = 300$ K and $T_d = 2500$ K. The model predicted a minimum noise figure of 1.5 dB with an associated gain of 7.8 dB at 60 GHz. The amplifier consists of three noise-matched identical stages. The matching circuits composed of short-circuited lines were optimized to be a compact layout area by choosing a gatewidth of 60 μm. Each stage was designed to be unconditionally stable by incorporating series feedback lines for the source terminal and *RC* bias networks for the drain terminal of the FET. At all frequencies, a stability factor $K > 2$ for the overall three-stage amplifier was realized. In order to keep HJFET layout symmetry with the series feedback lines, the source terminal of the HJFET was divided into two. Bypass capacitors were incorporated between the end of series feedback lines and the ground.

For the gate-bias network, the diode-regulated self-bias circuit discussed in Section II has been incorporated. A current limiting resistor and the diode were connected in series between the end of series feedback lines and the ground. The V_f is applied to the gate terminal of the FET through the matching circuit. With a drain current of 5 mA/stage at 3 V, the total dc power consumption was estimated to be 45 mW.

IV. FABRICATION PROCESS AND DEVICE CHARACTERISTICS

The cross-sectional view of an AlGaAs/InGaAs HJFET used in the monolithic LNA is shown in Fig. 7. The epitaxial layer

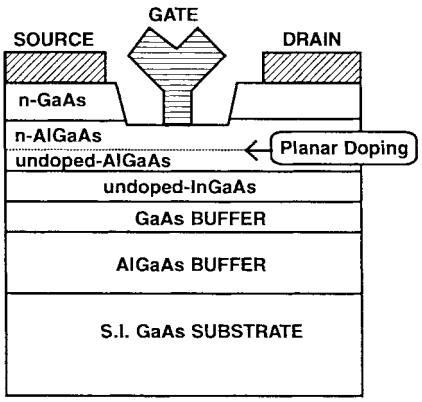

Fig. 7. Cross-sectional view for the AlGaAs/InGaAs HJFET.

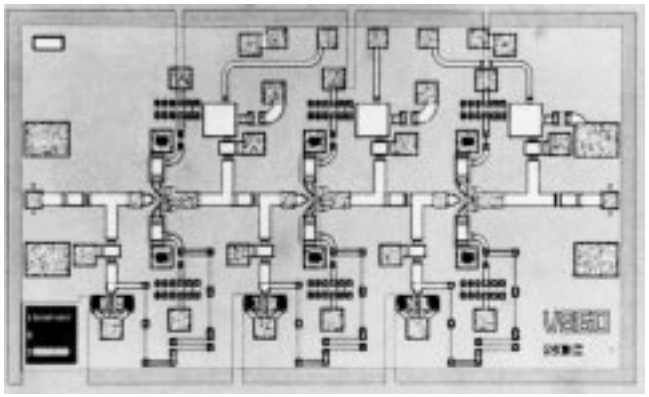

Fig. 8. Chip photograph for the single-bias three-stage monolithic LNA. Chip size is 1.85 × 1.07 mm^2.

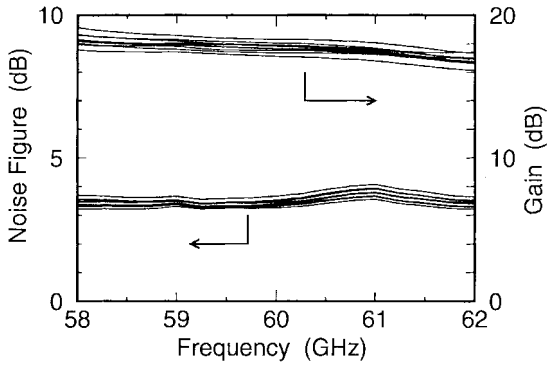

Fig. 9. Measured noise figure and gain of ten monolithic LNA's at 3 V.

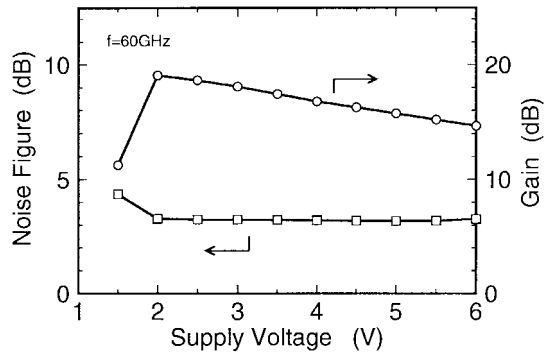

Fig. 10. Measured noise figure and gain at 60 GHz as a function of supply voltage.

structure for the HJFET consists of AlGaAs and GaAs buffer layers, a 13-nm undoped $In_{0.2}Ga_{0.8}As$ channel layer, a 33-nm $Al_{0.2}Ga_{0.8}As$ layer with 5×10^{12} cm^{-2} Si-planar doping, and an 80-nm n$^+$-GaAs cap layer.

In FET fabrication, mesa-isolation, wet recess etching, electron-beam evaporation, and lift-off techniques were employed. Details were reported elsewhere [6], [7]. A Schottky gate of the HJFET was used as a current regulating diode. A metal–insulator–metal (MIM) structure with an SiN film as a dielectric layer was applied for fabricating both dc blocking and bypass capacitors. N^+ bulk resisters were used in the bias networks.

The HJFET has a T-shaped gate with 0.15-μm length. The device exhibited a typical transconductance of 510 mS/mm and an $f_{\max}$ of 200 GHz at $V_{ds} = 2$ V with a reverse gate–drain breakdown voltage of 10 V. The measured minimum noise figure for the device was 0.4 dB at 12 GHz with an associated gain of 13 dB.

V. LNA Performances

The chip photograph for the three-stage MMIC LNA is shown in Fig. 8. The chip size is 1.85 mm × 1.07 mm × 0.04 mm. It corresponds to a chip size per stage of 0.66 mm^2/number, which is much smaller than that of our previous two-stage LNA (1.19 mm^2/number) [8], due to the matching circuit optimization and the self-bias circuit incorporation.

Ten MMIC chips were tested by on-wafer RF probes. Drain currents were at a range from 3.5 to 5.1 mA/stage for a supply voltage (V_d) of 3 V. The measured noise figure and gain as a function of frequency are represented in Fig. 9. Noise-figure variation at 60 GHz was from 3.2 to 3.7 dB and gain variation was from 17.2 to 18.3 dB. For the best chip, the average noise figure from 58 to 62 GHz was 3.3 dB with 18-dB gain.

The measured noise figure and gain of the LNA as a function of supply voltage are shown in Fig. 10. The LNA operated with a constant noise figure over 2–5 V. When the supply voltage was increased from 3 to 5 V, the drain current gradually increased only by 10%, with remaining 16-dB gain at 60 GHz.

Since V_f is affected by temperature, its dependence of LNA noise characteristics is interesting. The measured noise figure, gain, and bias current for the ambient temperature range of 20 °C ± 50 °C are shown in Fig. 11. The noise figure and gain variations were ±0.5 dB and ∓ 1.6 dB, respectively. The current deviation over a 100 °C temperature range for this circuit was 9%, which is the same level as a resistive self-bias network for a C-band LNA [3].

VI. Conclusions

Design and performance of a single-bias 60-GHz-band monolithic HJFET LNA were described. A diode-regulated self-bias circuit was incorporated to reduce the drain–current sensitivity to FET threshold voltage variations. The effect of the bias circuit on the drain–current distribution was analyzed

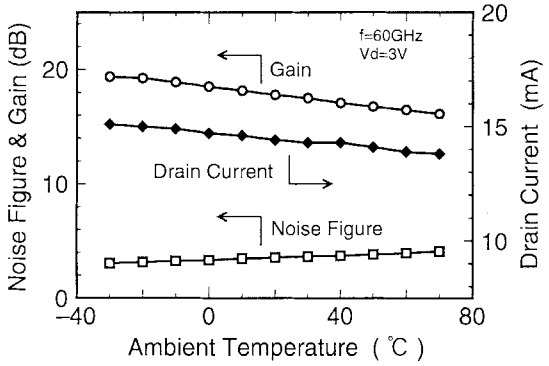

Fig. 11. Typical noise figure, gain, and drain current for the range from −30 °C to 70 °C.

based on the FET dc characteristics. For the best LNA, the average noise figure from 58 to 62 GHz was 3.3 dB with 18-dB gain at 3 V. The LNA operated with a constant noise figure over 2–5 V with a gain higher than 16 dB at 60 GHz. The developed MMIC LNA featuring a small chip size and an excellent noise performance as well as a single-bias supply with a wide voltage range promises great applicability to low-cost millimeter-wave wireless systems.

ACKNOWLEDGMENT

The authors wish to thank Y. Ando, K. Onda, M. Funabashi, and M. Kuzuhara for their useful discussions, and S. Hasegawa, T. Uji, and M. Ogawa for their support.

REFERENCES

[1] Y. Takimoto, H. Yatsuka, A. Inoue, T. Yokoyama, T. Aoyagi, K. Ohata, T. Saito, T. Negishi, and N. Okubo, "60 GHz short range transceivers and applications for minimum delay spread LAN," in *IEEE MTT-S Int. Microwave Symp. Dig.*, San Francisco, CA, June, 1996, pp. 509–512.

[2] B. Hughes, J. Perdomo, and H. Kondoh, "12 GHz low-noise MMIC amplifier designed with a noise model that scales with MODFET size and bias," *IEEE Trans. Microwave Theory Tech.*, vol. 41, pp. 2311–2316, Dec. 1993.

[3] K. W. Kobayashi, R. Esfandiari, B. L. Nelson, K. Minot, W. L. Jones, M. Biendenbender, R. Lai, K. L. Tan, and J. Berenz, "Monolithic regulated self-biased HEMT MMIC's," *IEEE Trans. Microwave Theory Tech.*, vol. 42, pp. 2610–2616, Dec. 1994.

[4] K. Hubbard, K. MacGowan, C. Kau, D. Smith, and S. Maas, "A family of low cost high performance HEMT MMIC's for commercial DBS applications," in *IEEE MTT-S Int. Microwave Symp. Dig.*, Orlando, FL, May 1995, pp. 1649–1652.

[5] M. W. Pospieszalski, "Modeling of noise parameters of MESFET's and HEMT's and their frequency and temperature dependence," *IEEE Trans. Microwave Theory Tech.*, vol. 37, pp. 1340–1350, Sept. 1989.

[6] Y. Nashimoto, Y. Makino, K. Onda, M. Kuzuhara, and K. Arai, "Super-low noise heterojunction field-effect transistors (HJFET's) with 0.2 μm T-shaped 8 gate-fingers," *NEC Res. Dev.*, vol. 33, pp. 268–272, July 1992.

[7] N. Samoto, I. Miura, Y. Makino, and K. Yamanoguchi, "Sub-0.1-μm T-shaped gate fabrication technology using mixing-layer sidewalls in a double-layer resist system," *J. Vac. Sci. Technol.*, no. B12(6), pp. 3673–3676, Nov./Dec. 1994.

[8] K. Maruhashi, M. Funabashi, T. Inoue, M. Madihian, and M. Kuzuhara, "A 60GHz-band low noise HJFET amplifier module for wireless LAN applications," in *IEEE MTT-S Int. Microwave Symp. Dig.*, San Francisco, CA, June 1996, pp. 13–16.

Kenichi Maruhashi (A'96–M'97) was born in Aichi, Japan, on February 11, 1967. He received the B.S. and M.S. degrees in physics from Kobe University, Kobe, Japan, in 1989 and 1991, respectively.

In 1991, he joined NEC Corporation, Otsu, Shiga, Japan, where he works on modeling, design, and characterization of HJFET's, and development of MMIC's based on their technologies. His current research interest includes microwave and millimeter-wave integrated circuits for high-speed wireless communication systems. He is currently an Assistant Manager of the Kansai Electronics Research Laboratory, NEC Corporation, Otsu, Shiga, Japan.

Mr. Maruhashi is a member of the Institute of Electronics, Information, and Communication Engineers (IEICE), Japan.

Keiichi Ohata (M'86) received the B.E. and M.E. degrees in electronic engineering from Kyoto University, Kyoto, Japan, in 1970 and 1972, respectively.

In 1972, he joined the Central Research Laboratories, NEC Corporation, Kawasaki, Japan, and was engaged in the research of ohmic contacts to GaAs, development of low-noise GaAs MESFET's, and research and development of microwave and millimeter-wave heterojunction devices. From 1991 to 1996, he was temporarily transferred to the Advanced Millimeter Wave Technologies Co. Ltd., Japan, where he was responsible for the research of 60-GHz-band MMIC's for short-range communication systems. He is currently a Senior Principal Researcher at Kansai Electronics Research Laboratory, NEC Corporation, Otsu, Shiga, Japan, where he conducts the research and development of millimeter-wave devices for multimedia communications.

Mr. Ohata is a member of the IEEE Microwave Theory and Techniques Society, the IEEE Electron Devices Society, the Institute of Electronics, Information, and Communication Engineers (IEICE), Japan, and the Japan Society of Applied Physics.

Mohammad Madihian (S'78–M'80–SM'88) was born in Tehran, Iran, on January 3, 1954. He received the B.Sc. degree from the Iran University of Science and Technology, Tehran, Iran, in 1976, and the M.Sc. and Ph.D. degrees from Shizuoka University, Hamamatsu, Japan, in 1980 and 1983, respectively, all in electronic engineering.

In 1983, he joined NEC Microelectronics Research Laboratories, Kawasaki, Japan, where he has worked on research and development of compound semiconductor device-based digital as well as microwave monolithic IC's. He is currently a Principal Researcher at NEC C&C Media Research Laboratories, where he conducts research and development of GaAs-based monolithic millimeter-wave IC's and BiCMOS-based RFIC's for high-speed wireless LAN and personal communications applications. He has authored or co-authored over 90 scientific publications including 43 IEEE journal/conference papers, and holds 20 patents on device and circuit applications.

Dr. Madihian was the recipient of the 1988 IEEE MTT-S Microwave Prize, holds six NEC Distinguished Achievement Awards and R&D Contribution Awards, and is cited in the *Who's Who in the World*, *Who's Who in Finance and Industry*, and *Who's Who in Science and Engineering*. He is currently serving on the IEEE GaAs IC Symposium Technical Program Committee, IEEE MTT-S International Microwave Symposium MTT-6 Subcommittee, IEEE RF IC Symposium Technical Program Committee, and International Electrical Overstress and Electrostatic Discharge Symposium Technical Program Committee.